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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

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MONDT, JOHANNES P	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/498,677
Filing Date: February 07, 2000
Appellant(s): STEINHOFF ET AL.

Robert N. Rountree, LLC
(Reg. No.: 39,347)
70360 Highway 69
Cotopaxi, Colorado 81223
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/17/08 appealing from the Office action mailed 6/11/07.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

An appeal has been filed on 9/16/08 in a related application with identical title and related subject matter, 10/926,916, "Bi-directional ESD Protection Circuit", with common inventors Roberts Steinhoff and Jonathan Brodsky, and the same assignee, Texas Instruments. An Examiner's Answer was mailed on 12/26/08.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect in that it fails to include a statement on cancelled claims 14-45. A correct statement of the status of the claims is as follows:

Claims 14-45 were canceled.

Claims 1-13 stand rejected and are being appealed.

Therefore, this appeal involves claims 1-13.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is deficient. 37 CFR 41.37(c)(1)(v) requires the summary of claimed subject matter to include: (1) a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number, and to the drawing, if any, by reference characters and (2) for each independent claim involved in the appeal and for each dependent claim argued separately, every means plus function and step plus function as permitted by 35 U.S.C. 112, sixth paragraph, must be identified and the structure, material, or acts described in the specification as corresponding to each claimed function must be set forth with reference to the specification by page and line number, and to the drawing, if any, by reference characters.

The brief is deficient because on line 5 of said Summary Appellant incorrectly identifies the substrate with reference character 171. This is incorrect. Instead, the reference character for the substrate on which the first transistor is formed is 172 while reference character 171 refers to a P-well region within said substrate (see Fig. 1C and page 5, lines 6-8).

The brief is additionally deficient because the substrate is also incorrectly identified with 108, which contradicts both the appeal brief itself and the specification,

because 172 is the substrate while 108 is a lead connecting gate and substrate of first transistor 106 (see Fig. 1A and page 4, lines 21-23).

Appellant repeats the same error with regard to his summary regarding the third transistor, wherein 108 incorrectly is used to denote the transistors' substrate instead of the correct reference character 172.

Appellant's comments in said Summary on operation (second paragraph in Summary) are superfluous for the instant device claims.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,369,457	WLLIAMSON	04-2002
6,060,752	WILLIAMS	05-2000
5,976,921	MAEDA	11-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a verbatim copy of the Grounds of Rejection as provided in the Office action as appealed (mailed 6/11/07), without any alternations intended:

BEGINNING OF GROUNDS OF REJECTION:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. ***Claims 1, 2, 6, 7, 11 and 12*** are rejected under 35 U.S.C. 102(e) as being anticipated by Williamson (6,369,427 B1) (previously made of record).

Williamson teaches a structure (Figures 5-6, col. 6, l. 17 – col. 7, l. 30) comprising:

an external terminal Vdd (e.g., Fig. 5 and col. 5, l. 14);

a reference terminal (ground) (Figure 5 and col. 5, l. 65-66);

a first transistor 56 (col. 6, l. 37-40) formed on a substrate (see jointly Figures 5-6), the first transistor having a current path electrically connected between the external terminal Vdd and the reference terminal (ground) (Figure 5);

a second transistor (p-type transistor in 44) having a current path electrically connected between the substrate (through node 66 and electrical connection with

resistor 42 connecting to a terminal common to the two transistors in 44: see Figure 5) (col. 6, l. 17-31);

a third transistor (n-type transistor in 44) having a current path electrically connected between the substrate (through node 66 and an electrical connection with resistor 42 connecting to a terminal common to the two transistors in 44: see Figure 5) and the reference terminal (ground) (see Figure 5) (col. 6, l. 17-31);

wherein the current paths of the second and third transistors are in parallel with the current path of the first transistor (namely: both are connections between Vdd and ground but running as parallel circuitry: see Figure 5).

On claim 2: the structure further comprises a first resistor (either the inherently present contact resistance caused by the contact made between the gate and the source/drain in said second transistor (p-type transistor in 44), or, in an alternative, resistor 42 (N.B.: note that 42 also is located between Vdd (see 46) and said current path of the second transistor) coupled between the external terminal and the current path of the second transistor; and a second resistor coupled between the current path of the third transistor (n-type transistor in 44) and the reference terminal (ground) (said second resistor being either resistor 42 or the contact resistance caused by the contact between the gate of said third transistor and the source/drain terminal closest to ground, respectively).

On claim 6: the first transistor 56 further comprises a control terminal (gate 67) (electrically, in particular: capacitively) coupled to the substrate (col. 6, l. 46).

On claim 7: the structure further comprises a first resistor (either the inherently present contact resistance caused by the contact made between the gate and the source/drain in said second transistor (p-type transistor in 44), or, in an alternative, resistor 42 (N.B.: note that 42 also is located between Vdd (see 46) and said current path of the second transistor) coupled between the external terminal and the current path of the second transistor; and a second resistor coupled between the current path of the third transistor (n-type transistor in 44) and the reference terminal (ground) (said second resistor being either resistor 42 or the contact resistance caused by the contact between the gate of said third transistor and the source/drain terminal closest to ground, respectively).

On claim 11: the structure further comprises a protected circuit 34 (col. 4, l. 27-47) electrically connected to the external terminal Vdd (Figure 5).

On claim 12: the first transistor 56 is a MOS transistor (NMOS transistor; see col. 6, l. 37-40) having a control gate 67 (col.6, l. 44-48) electrically connected to the substrate through capacitive coupling (any MOS transistor is a MOS capacitor and capacitive coupling meets “electrically connected”.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 3-5, 8-10 and 13*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Williamson as applied to claim 1 above, in view of Williams (6,060752).

On claims 3-4 and 8: As detailed above, Williamson anticipates claim 1. Williamson does not necessarily teach the further limitations defined by claims 3-4, or claim 8. However, it would have been obvious to include said further limitations in view of Williams, who, in a patent on a semiconductor-based ESD protection circuit (title, abstract), hence analogous art, teaches a lightly doped region as substrate 900, having a first type conductivity (p-type in Williams), a first heavily doped region (NBL region 926 or NBL region 928) having a second conductivity type (n-type in Williams) and underlying the substrate and the active region so as to suppress parasitic capacitance; and a second lightly doped region 904 having second conductivity type (n-type in Williams) formed at a face of the substrate and extending to the first heavily doped region. *Motivation* to include the teaching by Williams in the invention by Williamson derives from the resulting diode (D1) protection through the doping of the substrate, (b) additional protection provided by the well region 904 and (c) the suppression of parasitic capacitance through heavily doped buried region (926 or 928), which are advantages independent of the nature of the device operating through the active region. Note that this motivation holds for any of the transistors in the circuitry by Williamson.

On claim 5: in the combined invention the interface between 62 and 65 on the one hand, and the well region equivalent to 60 on the other hand form first and second

diodes coupled between the external terminal and the second lightly doped region (well region), and between the reference terminal and said second lightly doped region.

On claim 9: in the combined invention the region of substrate 60 is a lightly doped well of conductivity type opposite those of the diffusion regions. Therefore, first and second diodes are formed (60 appropriately modified to be lightly p-doped following Williams) as well as a second terminal 60 coupled between respectively the first and second resistor and the current path (channel) of respectively the second and third transistor (N.B.: all three channels themselves being coupled to each other).

On claim 10: the structure further comprises: an isolation circuit 36 (col. 5, l. 1-5; also col. 4, l. 20-25 and Figure 5) connected to the external terminal Vdd (Figure 5); and a protected circuit 34 (col. 4, l. 26-47 and Figure 5) electrically connected to the isolation circuit.

On claim 13: although Williamson does not necessarily teach the further limitation that the first transistor is a bipolar transistor having a base terminal electrically connected to the substrate, it would have been obvious to include said further limitation in view of Williams, who teach equivalence of MOSFET device based ESD protection circuitry and bipolar transistor based ESD protection circuitry in his invention (see col. 2, l. 50-55).

2. ***Claim 13*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Williamson as applied to claim 1, in view of Maeda (5,976,921).

As detailed above, claim 1 is anticipated by Williamson. Williamson does not necessarily teach the further limitation defined by claim 13. However, it would have been obvious also to include said further limitation in view of Maeda, who, in a patent on an semiconductor based ESD protection device (title, abstract), hence analogous art, teaches a ESD protection device based on MOS transistors and a bipolar transistor (see Example 1), wherein a base terminal is electrically connected to the substrate (abstract and col. 13, l. 48-65; P-well being the base; base contact 6aa providing the electrical connection to the substrate: see Figure 8 and col. 14, l. 40-52) so as to enable the escape of excessive current and voltage. *Motivation* to include the teaching by Maeda in this regard derives from the effectiveness of the bipolar transistor to protect against excessive current and voltage.

END OF GROUNDS OF REJECTION

(10) Response to Argument

Prior to responding to the specific arguments of appeal examiner herewith provides a mapping of the independent claim onto the prior art specification by means of the Drawings and column and line numbers.

Primary Reference: Williamson | Assignee: "VLSI Technology" | Effective File Date

U.S. Patent Apr. 9, 2002 Sheet 3 of 4 US 6,369,427 B1 Nov. 3,'98

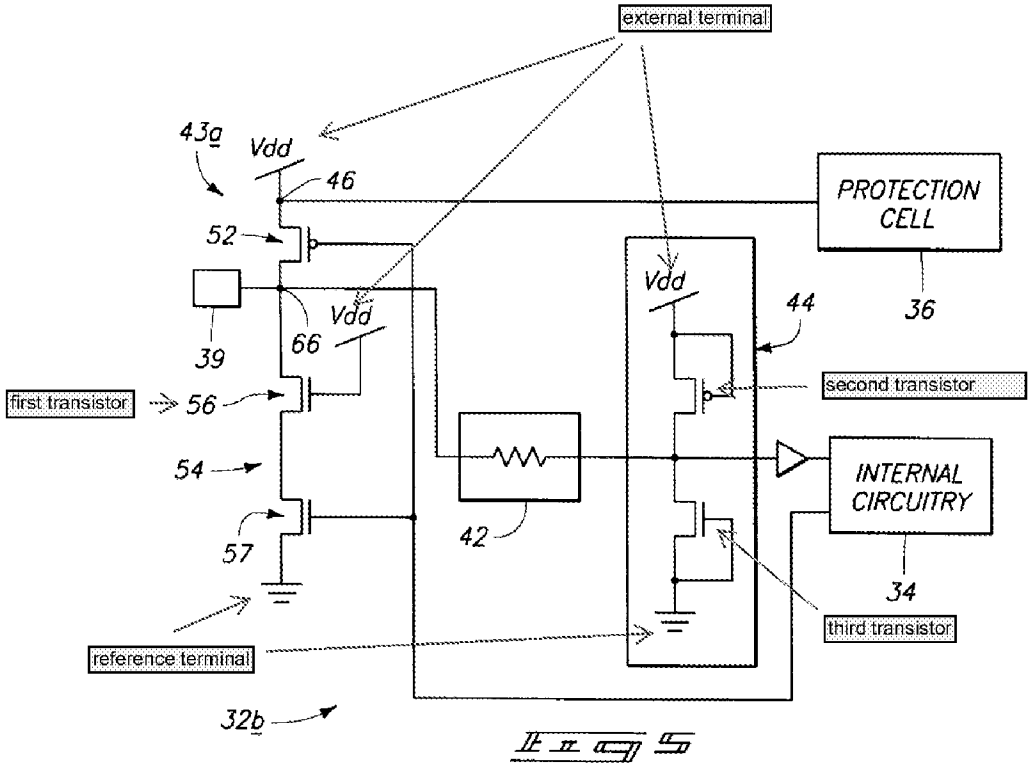

Fig 5

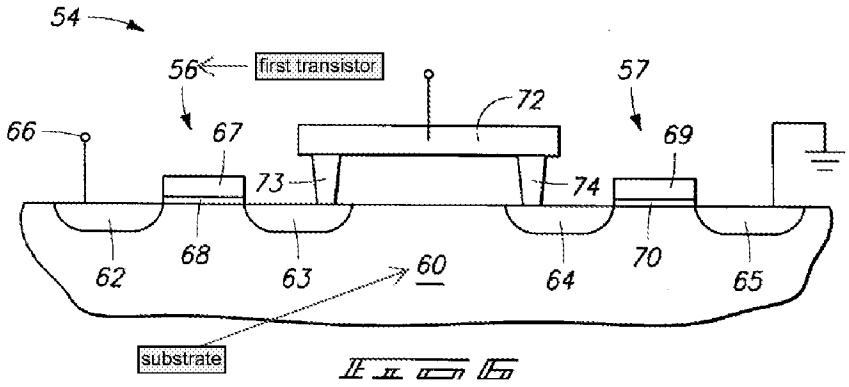

Fig 6

Regarding claim 1, and with reference to Figures 5 and 6, and col. 6, l., 17 – col. 7, l. 30, as reproduced with annotations by examiner,

- "an external terminal" is met by V_{DD} Figure 5 and col. 5, l. 14);

- "a reference terminal" is met by ground terminal (Fig. 5 and col. 5, l. 65-66);
- "a first transistor" is met by element 56 (Fig. 5, col. 6, l. 37-40) is formed on substrate, met by element 60 (see jointly Figs. 5 and 6; and col. 6, l. 35), the first transistor having a current path (through its channel between its source and drain) electrically connected between the external terminal V_{DD} and the reference terminal (see V_{DD} most to the left in Figure 5);
- "a second transistor" is met by the upper transistor in element 44 ('voltage clamp' as transistor pair: see col. 6, l. 25-26), which has a current path electrically connected between the external terminal V_{DD} (see right-most V_{DD} in Fig. 5) and the substrate 60, namely: through resistor 42, node 66 and source/drain region of said first transistor 56 (see Fig. 5 and col, 6, l. 17-30); and
- "a third transistor" is met by the lower transistor in said element 44, which has a current path electrically connected between the substrate 60 and the reference terminal (ground terminal shown to the right in Figure 5), namely: through the resistor 42, node 66 and source /drain region of the first transistor 56 (see Fig. 5 and col. 6, l. 17-30),
- while the current paths of the second and third transistors are in parallel with the current path of the first transistor 56, because both aforementioned current paths connect independently V_{DD} and ground (Figure 5).

The following is a list of appellants' arguments of appeal, with corresponding examiner's responses:

Ad A. Rejection under 35 USC 102(e) as anticipated by Williamson.

A.1: the independent claim 1:

1. *Applicants' first argument*: page 4, lines 3-15, alleging examiner did not properly address the limitation "between the substrate" in relation to second and third transistors.

Answer: Examiner disagrees because said first argument is merely reliant on an inadvertent omission of "between the substrate" in an otherwise integrally included claim language with comments: in an attempt to reproduce the entire text of the claim examiner inadvertently omitted the wording "between the external terminal" in line 2 of page 3 of the office action.However, included in the rejection is an explanation of the connection by which external terminal "through node 66 and electrical connection with resistor 42 connecting to a terminal common to the two transistors in 44": see Figure 5) (col. 6, l. 17-31). It had, prior to this point in the rejection, been made clear that V_{DD} is the external terminal. In Figure 5 of the reference (Williamson (US 6,369,427 B1)) the substrate is electrically connected to the source and drain regions within said substrate that inherently function as two of the three terminals of field effect transistor 56; the source and drain regions are located at the extreme ends of the regions of the substrate below the gate 67 (see Figure 6). So the question is whether there is an electrical connection between the source/drain region on the upper end of the transistor 56 through node 66 and resistor 42 to terminal VDD through the current path of p-type

(dotted) transistor in element 44 (Figure 5). Examiner further disagrees with applicant because this electrical connection is plainly evident.

2. *Appellants' second argument*: on page 4, lines 3-23; appellant contests a statement on capacitive coupling allegedly being included in examiner's understanding of what may be interpreted to meet the limitation "electrically connected"; in particular "Examiner has interpreted substrate connections recited in claim 1 as capacitive coupling between source and drain regions of the p-type and n-type transistors in 44".

Answer: Examiner disagrees because:

(a) the relevance with regard to the grounds of rejection of independent claim 1 is absent. Appellants refer to page 7 of the Final Office action as appealed, yet page 7 does not contain any portion of the rejection of claim 1; while

(b) even if such statement would have been made in said rejection of claim 1, and even if, arguendo, the rejection would have relied on said statement, said statement would have been fully correct: any text book on electrical circuits including high school text books would easily confirm that electrical components may be connected electrically through (a) resistors, (b) inductances and / or (c) capacitances, and in all of the above three cases, an electrical connection is established. In the OFF state of transistor 56 only the capacitive electrical connection exists, but in the ON state a channel in the substrate created by the action of the particular voltage on the gate carries the electrical current through the transistor and forms the current path.

3. *Appellant's third argument:* in the paragraph bridging pages 4 and 5, appellants allege that "[N]either the p-type transistor nor the n-type transistor in 44 of Williamson

has a current path electrically connected between the external terminal and the substrate", arguing that "[i]f capacitive coupling between source/ drain regions and the substrate of Williamson is taken as the current path recited in claim 1, then the current paths of the second and third transistors are not in parallel with the current path of the first transistor, which is electrically connected between the external terminal and the reference terminal".

Answer: Examiner disagrees, because the p-type transistor indeed has such current path as discussed above, i.e., through the channel; while even *arguendo*, appellant's argument on capacitive coupling is entirely incorrect, because (a) the rejection of claim 1 does not rely on capacitive coupling while (b) said capacitive coupling would then apply to all transistors including those in element 44.

4. *Appellants' fourth argument*: on page 5, second and third full paragraphs, once again relies on the same issue of capacitive coupling.

Answer: appellants' argument is based on a full misunderstanding of the rejection in the Final Office action. Again: examiner does not rely in any manner on the interpretation of capacitive coupling as meeting "electrically connected", although for the reasons exactly as discussed above examiner maintains the correctness of such interpretation.

A.2: Dependent claims:

On claims 2 and 7, appellants' argument (paragraph bridging pages 5 and 6, and for claim 7 the second full paragraph of page 6) rejects the contact resistance caused by the contact between gate and source/drain in second and third transistors as being a

"resistor", argues further that therefore only resistor 42 is available for both first and second resistor, by which the rejection is appealed.

Answer: examiner disagrees, because "contact resistance" is a narrower term of resistance and any feature increasing the resistance is, to anyone skilled in the art, a resistor. Specifically, the connections through an electrical lead between the gate and the source/drain regions closest to the closest terminal marked V_{DD} in Figure 5 is not generic to all field effect transistors and inherently represents a true contribution to the total resistance of the external terminal V_{DD} and the current path (between source and drain) of the p-type (doted) transistor in element 44. Accordingly, resistor 42 is not the only resistor coupled between the external terminal and the current path of the second transistor. Similarly, the contact resistance due to the lead between the gate and the source/drain region in the third transistor meets the limitation "resistor", and is a resistor coupled between its current path and the reference terminal. In addition, resistor 42 is a resistor coupled between the external terminal V_{DD} (through node 66) and the current path of the second transistor, as well as coupled between the current path of the third transistor and the reference terminal (see the ground terminal on the left in Figure 5). Clearly, the resistances from the current path (channel) of second transistor and third transistor to external and reference terminals are not the same and represent resistors that respectively meet the limitations "first resistor" and "second resistor", whether taken as a whole or in separate partial contributors to said resistors.

On claims 6 and 12, appellants' argument (first and third paragraphs of page 6) is exactly the previously discussed argument against the interpretation of capacitive

coupling as meeting “electrically connected”. Counter to appellants’ argument that “examiner again resorts to” this argument, these claims are the only claims of which the rejections rely on such interpretation. Examiner refers to the above discussion of appellants' arguments in appeal of claim 1, in particular answer ad A.1, 2 (b), herewith included by reference in its entirety. Counter to appellants' argument that capacitive coupling if interpreted as electrical connection would render it impossible to draft claims, the Honorable Board may have understanding for the availability of descriptions such as "resistively connected", "capacitively connected", "inductively connected"; while, on the other hand, after adoption of appellants’ terminology to facilitate claim drafting, a circuit in which a capacitor is interposed between two other electrical elements would imply the absence of an electrical connection between said other elements through said capacitor, and hence all text books with capacitor-comprising circuits would have to be scrutinized for re-editing.

Ad B. Rejection under 35 USC 103(a) as being unpatentable over Williamson in view of Williams:

1. *Appellants' first argument* (page 7, first paragraph) is that claim 4 is patentable because “no first transistor is formed on substrate 900 of Williams”.

Answer: examiner disagrees with said first argument because the rejection did not rely on the existence of a first transistor in Williams, but instead on whether the diode protection through doping of the substrate (substrate 900 is lightly p-doped in its upper portion 902) and first and second lightly doped regions 926 and 928 of the opposite conductivity type (n-type) in an ESD device substrate offers added protection

that would have been obvious also for the ESD protection device of Williamson. Williamson and Williams clearly are analogous art, both drawn to substrates for ESD protection. Williamson teaches the first transistor. Williams is not cited for said first transistor.

2. *Appellants' second argument* (page 7, first paragraph) is that claim 4 is patentable because 926 and 928 are not under substrate 900.

Answer: Examiner disagrees because, in light of the specification, the "substrate" as disclosed is not analogous to a doped well sub-region within the substrate counter to Appellant's "Summary of the Claimed Subject Matter" (see section 5 of this Examiner's Answer), - although such doped wells can by themselves be interpreted as substrates; but instead as disclosed is the substrate layer 172. Obviously, only its upper portion 902 in Williams directly supports the transistors and is considered included within the meaning of substrate by one of ordinary skill in the art. Parenthetically, upper substrate portion 902 could easily have been singled out on its own to meet the limitation of substrate based on location and support provided to the transistors. Because of the light p-type doping of portion 902 the substrate also meets lightly p-type doped, while 926 and 928 are underlying said substrate in two different meanings: 926 and 928 are underneath the relevant portion 902 of 900 serving as substrate support for the transistors while being "hidden beneath the surface" of said substrate as a whole.

Ad C: Rejection of claim 13 under 35 USC 103(a) as being unpatentable over Williamson in view of Maeda:

1. *Applicants' first argument* (page 7) is that the BiCMOS process is incompatible with the CMOS process of Williamson.

Answer: Claim 13 is drawn to a structure, not a process. Furthermore, Maeda himself shows that MOS transistors, as also disclosed in Williamson, and bipolar transistors can both be combined in an ESD protection device substrate. Therefore, the structures in the proposed combination are utterly combinable in light of the references over which claim 13 is rejected.

2. Applicants' second argument (page 8) alleges "no teaching or suggestion in either reference to indicate how or why the second and third series-connected transistors of claim 13 might have current paths connected to the base of the first transistor and in parallel with a current path of the first transistor".

Answer: Examiner disagrees: No modification other than the selection of another kind of transistor, but performing the same function, is involved according to claim 13. In the combination, current paths of both types of transistor (field effect and bipolar) still run between source and drain, and hence no changes occur in the claimed properties of the current path when replacing a MOS or other field effect transistor with a bipolar transistor.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Johannes P Mondt/
Primary Examiner, Art Unit 3663

Conferees:

Jack W. Keith

/J. W. K./

Supervisory Patent Examiner, Art Unit 3663

Marc Jimenez

/MJ/

TQAS TC 3600